World of Computer Science and Information Technology Journal (WCSIT)
ISSN: 2221-0741
Vol. 1, No. 5, 235-238, 2011

FPGA Based Design and Implementation of Efficient Video Filter

[1]Rajesh Mehra
Faculty of ECE Department
NITTTR
Chandigarh, India
[1]rajeshmehra@yahoo.com

[2]Virendra Arya, [3]Rajpati Yadav
[2] Principal, DN Polytechnic
[3] Faculty of EI Department
[2, 3] Meerut, India
[3]rajsuchitra.yadav@rediffmail.com

Abstract— In this paper an efficient design and implementation of ITU-R BT.601 video filter has been presented for digital television receivers. The proposed video filter has been realized using MAC algorithm. The implementation is based on efficient utilization of embedded multipliers and look up table (LUT) of the target device to improve speed, area efficiency and power consumption. It is an efficient method because the use of embedded resources not only increases the speed but also saves the general purpose resources of the target device. The proposed video filter has been designed and simulated using Matlab, synthesized with Xilinx Synthesis Tool (XST), and implemented on Spartan 3E based 3s500efg320-5 FPGA device. The developed video filter structure can operate at an estimated frequency of 28.758 MHz by utilizing 12 multipliers and 245 LUTS of target FPGA device to provide cost effective solution for mobile and wireless communication systems.

Keywords-FPGA; ITU-R; LUT; Video Filter; XST.

I. INTRODUCTION

In the recent years interest and demand for real-time video has increased in many application areas. For example real-time digital video is used in video conferencing, surveillance and remote vehicle guidance systems. The traditional hardware implementation of image processing uses Digital Signal Processors (DSPs) or Application Specific Integrated Circuits (ASICs). The growing need for faster and cost-effective systems triggers a shift to Field Programmable Gate Arrays (FPGAs), where the inherent parallelism results in better performance [1] -[3]. When an application requires real time processing, like video or television signal processing or real-time track computation of a robotic manipulator, then specifications are typically very strict and are better met when implemented in hardware [4]. Features like embedded hardware multipliers, increased number of memory blocks and system-on-a-chip integration enable video applications in FPGAs that outperform conventional DSPs [5]. The continual growth in the size and functionality of FPGAs over recent years has resulted in an increasing interest in their use not only as testing platforms prior to CMOS implementation, But as fully working systems in their own right. There is particular interest in their use for image processing applications especially real-time video processing due to the potential of creating parallel processing architectures [6].

FPGA technology has reached such a level as to become attractive implementation architecture for RTVPS (Real-time Video Processors). Features such as distributed and block memory structures enable efficient implementation of line buffering in video processing operators. *Crooks* and Norell present two similar methods for the implementation of these kinds of systems [7, 8]. Neither of these two works presents a formal description of the allocation task they claim to solve. Nor do they fully utilize the capability of modern FPGA memory architectures. The Xilinx Spartan 3 architecture offers dual ported block-RAMs (Random Access Memory). This feature will allow two data arrays to share the same block-RAM without time scheduling. Computationally demanding functions like filters to control brightness, contrast, edge detection, smoothening, gray scale, and scaling are better optimized when targeted on FPGAs [9]- [10] . The main problems in real-time video filtering are synchronization, memory usage and delay. They are directly related to cost of the filter [11].

The filter design varies on different color spaces and application of the filter. Color space conversion inside the design provides more flexibility and reliability to the design [12] - [14]. The main color spaces used in the real-time video filter implementation are RGB (Red, Green, and Blue) and

YCbCr (Luminance, Chrominance). The advantages of parallel and pipelined processing of the filters are speed and easy synchronization of total design [15, 16]. Usually each filter is designed for specific function so for some application more than two filters are needed; therefore serial connected parallel control filter chain is used for better performance. Introduction of neighboring filter method increase the smoothness, sharpness and edge detection to the real-time video. The video character/text overlay generator [17, 18] is suitable for the display of closed caption or subtitles, user menus, status or error information, time-code or channel identifiers. The character generator structure contain a character ROM, keyboard interface circuit and display control, all these blocks are working parallel.

II. VEDIO FILTER

With the rapid development of computer technology, digital processing technology and image compression technology, the development of digital television (DTV) draws popularization of the sun at high noon. In the television signal processing, the digital filter plays an important role. Digital filter can complete the various roles played by analog filters, and have better performance. Such as: limiting the band in the signal receiving circuit, enhancing high-frequency signal, extracting high-low frequency signals (image profile signal extraction), separating the brightness and chrominance signal, demodulating chrominance signal and so on, such as the extraction of inter-frame filtering surface moving map information, dynamic signal balance, the elimination of fringe signal, audio signal compression processing. In these video images and audio signal processing systems, all require real-time signal processing and flexibility.

In the existing DSP processor at the same time, it is difficult to achieve these two requirements. In today's market, it can quickly and easily to the actual realization of the theoretical design of the Field-Programmable Gate Array (FPGA) technology to achieve more and more large-scale integrated circuits used in the design of modern digital electronic products, such as : digital TV technology. Video Filter is used to reduce noise from real time moving pictures. It improves visual quality by smoothing the sharp edges. The real-time digital video is used in video conferencing. The filters are used to control brightness, contrast, edge detection, smoothening. The Filtering are better optimized when targeted on FPGA. The memory usage is directly proportional to the cost and power consumption of the design. The real-time application consumer always looks for small memory usage design.

FPGA technology allows the realization of convenient filter design and simulation. And its relatively low price, compact size and efficient operation cut down the costs, reduce system size and weight, improve efficiency and performance. Therefore, the use of FPGA technology to design IIR filter has a broad meaning and long-term prospects of today's digital filter. At present, the realization of digital filters can be used in two ways: the software and hardware implementation. The software implementation means use software to achieve with micro-computer. Software packages for signal filtering in different languages have released by research institutions and Companies at home and abroad. But this method is slow and difficult to real-time signal processing. Although it can be used Fast Fourier Transform algorithm to speed up the computing speed, the real-time processing is achieving a very high price to pay. So it is usually used in teaching and research work. The hardware implementation means use dedicated hardware to design digital filter. Now, Programmable Logic Device (PLD) have made great advance in density, performance, power consumption and cost. It has stimulated a new line of digital signal processing and made the digital signal processing system based on software be flexible. In the foreseeable future, FPGA will rule more application fields.

III. PROPOSED VIDEO FILTER DESIGN

The ITU-R BT.601video filter has been designed and simulated using Matlab by using the concept of L^{th} band filtering. The designed video filter is a low-pass filter with a -3 dB point at 3.2 MHz, sampling frequency of 13.5 MHz. The passband ripple and stopband attenuation range has been specified as per ITU standard.

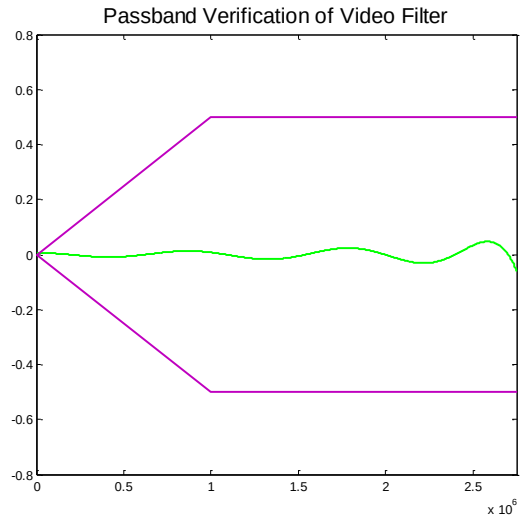

Figure 1: Video Filter Pass Band

The halfband video filter has been designed where every other coefficient is zero with the exception of the coefficient at the filter midpoint. The stop band attenuation and pass band ripples of developed filter have been compared with ITU-R BT.601 specifications. The red lines show the allowed variation in the specification. In Fig.1, purple line shows the ITU specification for pass band ripples and green line shows the pass band ripples of developed filter which is well within the specified range.

Similarly in Fig.2, purple line shows the ITU specification for stop band attenuation and green line shows the stop band attenuation of developed video filter which is well within the specified range.

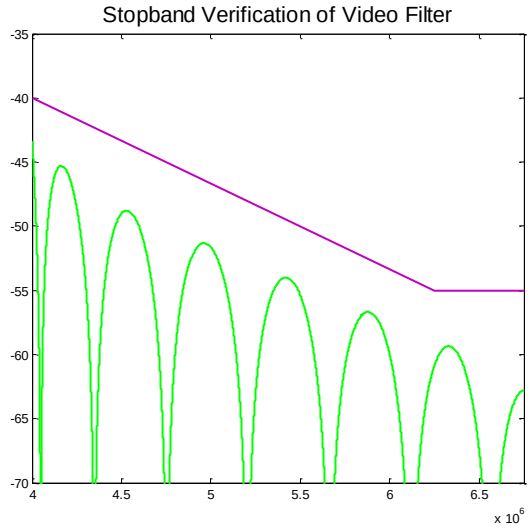

Figure 2: Video Filter Stopband

Then the developed video filter has been quantized by using suitable number of bits for input, output and for coefficients to meet the desired ITU specifications. The stimulus data for developed video filter contains impulse, step, ramp, chirp, and noise inputs as shown in Fig.3.

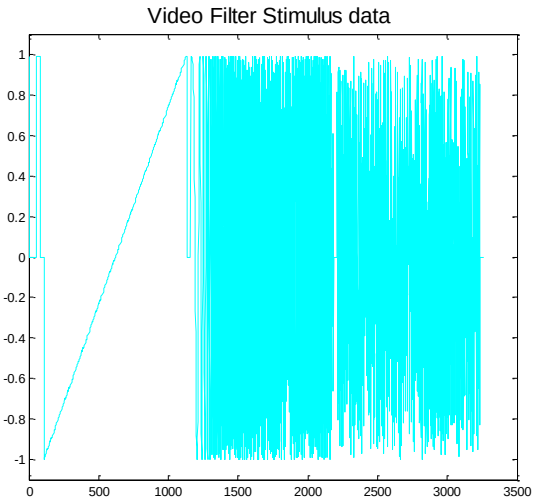

Figure 3: Stimulus Data

IV. H/W Implementation Results & Discussions

Nyquist video filter provide same stop band attenuation and transition width with a much lower order. An *L*th-band Nyquist filter with $L = 2$ is called a half-band filter. The transfer function of a half-band filter is thus given by:

The proposed MAC algorithm based video filter can operate at a maximum operating frequency of 28.758 MHz as compared to 27 MHz in case of existing design [18]. The

$$H(z) = \alpha + z^{-1}E_1(z^2) \tag{1}$$

with its impulse response as

$$h[2n] = \begin{cases} \alpha, & n = 0 \\ 0, & \text{otherwise} \end{cases} \tag{2}$$

In Half band filters about 50% of the coefficients of $h[n]$ are zero. This reduces the computational complexity of the developed video significantly. The proposed video filter has been designed and implemented using MAC algorithm by efficiently utilizing the embedded multipliers and LUTs of FPGA Target device. The MAC based video filter design has been synthesized and implemented on Spartan-3E based 3s500efg320-5 target device and simulated with modelsim simulator. The modelsim simulator based output response of proposed video filter has been shown in Fig.4. Table 1 show the area, and speed comparison of designed video filter with existing design [18].

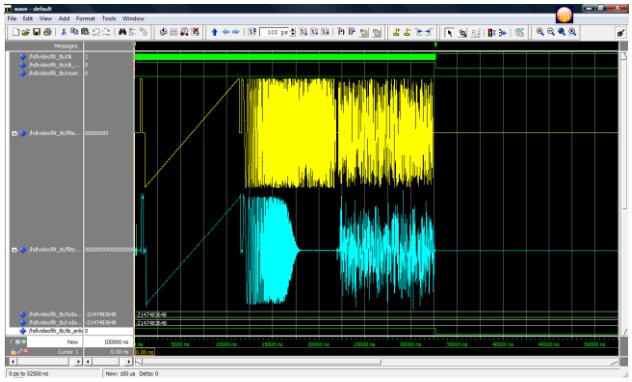

Figure 4: Modelsim based Video Filter Response

TABLE 1: AREA & SPEED COMPARISON

Logic Utilization & Speed	Existing Results [18] Used/Available	Proposed Results Used/Available
Number of Slices	1259/7680	246/4656
Number of 4 input LUTs	1464/15360	245/9312
Number Slice Flip-Flops	1289/15360	236/9312
Number of MULT18x18s	9/24	12/20
Number of BRAMB16s	6/26	-
Number of BUFGMUXs	4/8	-
Number of DCMs	3/4	-
Number of GCLKs	-	1/24
Video Frequency	27MHz	28.758MHz
Power Utilization	0.14453W	0.081W

proposed multiplier less interpolator has consumed only 246 slices, 236 flip flops and 245 LUTs and 12 multipliers available

on target device which is considerably less as compared to existing design [18].

V. CONCLUSION

In this paper, an area and power efficient video filter has been presented for digital television receivers. A video filter for ITU-R BT.601 has been designed and implemented on target FPGA device using MAC algorithm. The embedded multipliers and LUTs of target device have been efficiently utilized to enhance the speed and to provide the area efficiency. The results have shown enhanced performance in terms of speed, resource and power consumption. The proposed MAC based design can be operated at an estimated frequency of 28.758 MHz as compared to 27 MHz in case of [18]. The proposed video filter has consumed 246 slices, 236 flip flops and 245 LUTs and 12 multipliers. The total power consumption of the developed filter is 0.081W.

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AUTHORS PROFILE

Rajesh Mehra: *Mr. Rajesh Mehra is currently working as Faculty member of ECE Department at National Institute of Technical Teachers' Training & Research, Chandigarh, India. He is pursuing his PhD from Panjab University, Chandigarh, India. He has completed his M.E. from NITTTR, Chandigarh, India and B.Tech. from NIT, Jalandhar, India. Mr. Mehra has 15 years of academic experience. He has authored more than 30 research papers in reputed International Journals and 45 research papers in National and International conferences. Mr. Mehra's interest areas are VLSI Design, Embedded System Design, Advanced Digital Signal Processing, Wireless & Mobile Communication and Digital System Design. Mr. Mehra is life member of ISTE.*

Virendra Arya: Mr. Arya is working as Principal, D.N. Polytechnic. Mr, Arya's interest areas are Basic Electronics, Digital Electronics, Industrial Electronics & Control and Microprocessor.

Rajpati Yadav: Mr.Rajpati Yadav is currently working as Sr. Lecturer in ECE Department at Radha Govind Group of Institution, Meerut. *He has completed his B.Tech. From J.K.Institute of applied Physics and Technology, Allahabad University, India and pursuing M.Tech from NITTTR Chandigarh, India. Mr. Yadav has 9 years of academic experience.*